Advanced Design, Analysis and Verification of NoC Architectures

Abstract

Communication fabrics are critical for the quality (correctness, performance, energy, reliability) and fast integration of future computer systems in all segments. Examples of communication fabrics range from high-end regular rings and meshes in high-end servers and high-performance computing to SoC interconnect and IO fabric. Interconnect design is one of the greatest challenges faced by designers regardless of whether the interconnect fabrics are regular or irregular in structure.

Designing communication fabrics is a multidimensional challenge that involves complex functional and performance validation, cost analysis (area, power, design cost), and multilayered optimization (logical performance of interconnect vs. physical design aspects of the chip). This tutorial will summarize the results of the Communication Fabrics research program funded by Intel University Research Office and executed by multiple universities in collaboration with Intel Corp. In particular, the tutorial will cover:

- Functional correctness (memory consistency proofs, deadlock-freedom, livelocks)
- Traffic models for the evaluation of communication fabrics
- Quality of service analysis and optimization
- Uncore, interconnect, and system power management
- Physically-aware performance and area optimization for communication fabrics

Past Versions

The research activities that will be summarized in this tutorial are the outcome of the Communication Fabrics research program funded by Intel University Research Office. Intel Corp. held annual workshops between 2012 and 2014 to overview the funded research, provide feedback and coordinate the activity of different groups. These annual workshops were organized at Intel Oregon site, and they were limited to Intel employees and university participants of the research program. Each had around 50 local and remote attendees. This tutorial will be the first one that will be open to public.

Rationale for the Event and Collocating with PACT

Three years of collaborative research between six universities and Intel Corp. generated significant amount of research outcome. While some pieces of this research have been presented by participants in different venues over the last four years, the combined vision and major highlights have not been presented in a conference or workshop before.

The proposed tutorial is a natural fit for collocating with PACT. Communication fabrics form the backbone of parallel architectures. With the move to chip-multiprocessors, on-die communication fabrics have become an essential component of current parallel architectures. Their functional correctness, performance and power efficiency, and accurate modeling are key components of current and future parallel systems.

Organizers

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Michael Kishinevsky, Strategic CAD Labs, Intel Corp.
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Diana Marculescu, Carnegie Mellon University
Umit Y. Ogras, Arizona State University
Julien Schmaltz, Eindhoven University of Technology

Event Format and Expected Number of Participants

We propose a half-day tutorial which will start with a general overview of communication fabrics, design challenges and major research vectors that will be covered. This will be followed by 40-minute presentations by 6 university participants listed under the organizers. The event will conclude with 15-minute Q/A session.

There will be seven presenters and one moderator in this tutorial. We expect to have around 40 attendees overall.